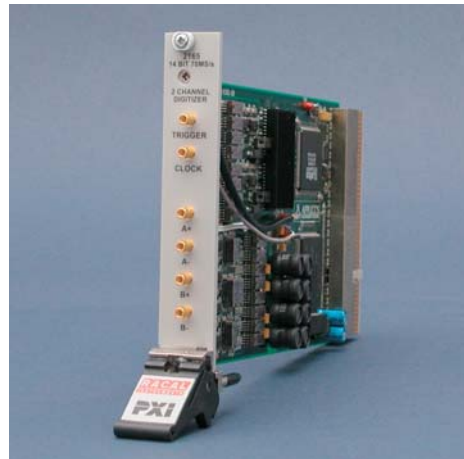


2 Channel, 14-Bit, 70 MS/s, PXI Digitizer Model 2165



- ◆ Two Independent Analog Input Channels, Single-Ended or Differential
- ◆ 14-bit Resolution per Channel
- ◆ Pre-Installed LabView™ and LabWindows™ libraries
- ◆ External or Internal Triggering
- ◆ Easy-to-Use Soft Front Panels
- ◆ Fully Supported VISA and Kernel drivers

Complete Signal Acquisition

Model 2165 is a high-performance, single-slot, two-channel, PXI-based digitizer. It has true dual channel performance, including separate user-selectable triggering and clock frequency for each channel.

Maximum Independence and Control

To provide maximum control while maintaining the unit's dual channel flexibility, the 2165 allows for signal acquisition either with or without triggering. Triggering can be either software-initiated or front-panel controlled, allowing each channel to start from different sources. For trigger inputs, Model 2165 accepts PXI back-plane sources, including PXI Trigger 1 to 5 or PXI STAR Trigger, as well as normal TTL signals from the front-panel connector, with positive or negative polarity, and edge or level triggering.

Complementing the unit's flexible triggering is the capability of selecting either an external clock source or utilizing the available 70 MHz or 50 MHz internal clock.

With easy-to-use soft front panels, reliable signal acquisition, non-triggered signal capture, and accurate signal analysis in time and frequency domains, Model 2165 is the natural choice.

Model 2165 comes with pre-installed LabView™ and LabWindows™ libraries, and supports VISA and Kernel drivers.

To ensure continued, uninterrupted, and reliable performance, Model 2165 can be user-calibrated with the supplied software.

Soft Front Panel Control

Soft front panels control the unit's settings for signal acquisition and for analyzing the acquired signal. Multiple graphs display in a single window, and one can zoom in or out of the viewed area. All results can be either selected or deselected with the active cursor.

Wealth of Features

The unit has a wealth of features for signal acquisition, including selection of the number of samples to be read and analyzed, trigger source and mode, continual signal capture mode (loop

mode), input offset voltage, clock source and frequency, and filtering type. All settings can be stored and recalled from the memory.

Model 2165 displays the acquired signal and the results of time domain and frequency domain analysis. In the time domain, one can display samples or a time axis. Frequency domain analysis offers windowing such as Hanning, Hamming, Flat-Top, Blackman-Harris, and others. Windowing is most beneficial when analyzing signals having a non-integer number of periods or when analyzing just part of the signal. Also, in the frequency domain, a summary of the harmonics is available. One can set the frequency domain settings as needed to ensure complete and accurate analysis and display, including Y-scale (auto, min, max, fixed), Reference (carrier, full scale of device, custom), and Spectrum (only the displayed content is taken into account for the parameter calculations). Lastly, the parameters SINAD, ENOB, THD, SNR, and Peak distortion are calculated and displayed.

2165 SPECIFICATIONS

PERFORMANCE

ADC Resolution

14-bits each channel

Sample Rate

Internal Clock:
500 kHz to 70 MHz

Absolute Accuracy (INL)

$\pm(500 \mu\text{V} + 0.1\% \text{ of range})$
With attenuator on:
 $\pm(2.5 \text{ mV} + 0.2\% \text{ of range})$

Relative Accuracy

$\pm 0.025\%$ of range

DC Offset Voltage

-5 V to +5 V
With attenuator on:
-25 V to +25 V

Clock Sources

Internal: 70 MHz or 50 MHz
External: Front panel connector

External Clock Input

Logic Thresholds: $V_{\text{LOW}} < 0.6 \text{ V}$
 $V_{\text{HIGH}} > 4.5 \text{ V}$

Impedance: 50 Ω
Maximum Input: 100 MHz

External Clock Output

Clock Levels: $V_{\text{LOW}} < 0.6 \text{ V}$
 $V_{\text{HIGH}} > 4.5 \text{ V}$

Impedance: 50 Ω

Clock Division Rate

User-selectable from 1 to 256
Independent clock source selection
per channel

Clock Accuracy

100 ppm

Memory Depth

512 k-words per channel

Frequency Response

(Referenced at 500 kHz)
0 to 20 MHz ($\pm 0.5 \text{ dB}$)
20 MHz to 50 MHz ($\pm 2.0 \text{ dB}$)

TRIGGERING

External Sources

Impedance: 10 k Ω DC
Levels: $V_{\text{LOW}} < 0.6 \text{ V}$
 $V_{\text{HIGH}} > 2.4 \text{ V}$

Internal Sources

PXI STAR
PXI TRIG 0 to 5
Software Trigger, Analog
(Independent trigger source selection
per channel)

Polarity

Positive
Negative

Response

Edge
Level, Continuous

INPUTS

DC Offset Range

Normal: -5 V to +5 V
With attenuator on: -25 V to +25 V

Ranges

Normal:
1 V (p-p)
2 V (p-p)
4 V (p-p)
With attenuator on:
5 V (p-p)
10 V (p-p)
20 V (p-p)

Filters

None
30 MHz
15 MHz
6 MHz
(3-pole Butterworth)

SFDR ($f_s = 50 \text{ MHz}/V_{\text{IN}} = 2 \text{ V(p-p)}$)

80 dB @ $f_{\text{IN}} = 1 \text{ MHz}$
72 dB @ $f_{\text{IN}} = 10 \text{ MHz}$

SINAD ($f_s = 50 \text{ MHz}/V_{\text{IN}} = 2 \text{ V(p-p)}$)

68 dB @ $f_{\text{IN}} = 1 \text{ MHz}$
64 dB @ $f_{\text{IN}} = 10 \text{ MHz}$

Channel Crosstalk

<70 dB @ 1 MHz

MAXIMUM CURRENT CONSUMPTION

+3.3 VDC 300 mA
+5 VDC 650 mA
-12 VDC 40 mA
+12 VDC 40 mA

FRONT PANEL INPUTS

Bandwidth (-3dB, filter off)
70 MHz

Coupling

DC
AC
Connector
SMB

Impedance

 (Selectable)

50 Ω AC-coupled
50 Ω DC-coupled
10 K Ω DC-coupled
Input Configuration
Single ended
Differential

ENVIRONMENTAL

Temperature

Operating: 0° C to 50° C
Storage: 0° C to 70° C

Relative Humidity

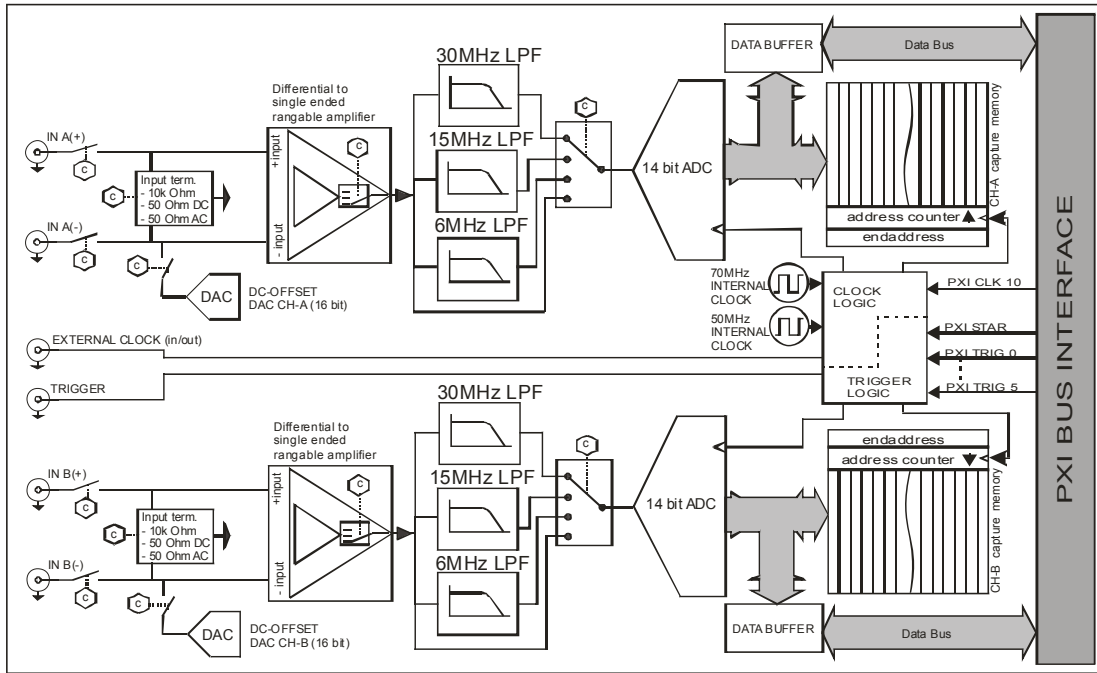
10% to 80%, non-condensing

Weight

7.4 oz. (210 grams)


Module Dimensions

3 U high, Single width



2165 FUNCTIONAL BLOCK DIAGRAM

ORDERING INFORMATION		
Model	Description	Part Number
2165	70 MS/s, 14-bit, 2-channel Digitizer	407946

 The CE Mark indicates that the product has completed and passed rigorous testing in the area of RF Emissions, Immunity to Electromagnetic Disturbances and complies with European electrical safety standards.

The Racal policy is one of continuous development; consequently, the equipment may vary in detail from the description and specification in this publication.

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